



Dual N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
40	0.032 at V _{GS} = 10 V	6 ^e	5.5 nC
	0.039 at V _{GS} = 4.5 V	5 ^e	

FEATURES

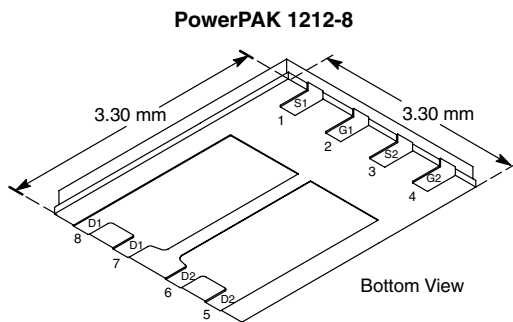
- TrenchFET® Power MOSFET
- Low Thermal Resistance PowerPAK® Package with Small Size and Low 1.07-mm Profile
- 100 % Rg and UIS tested



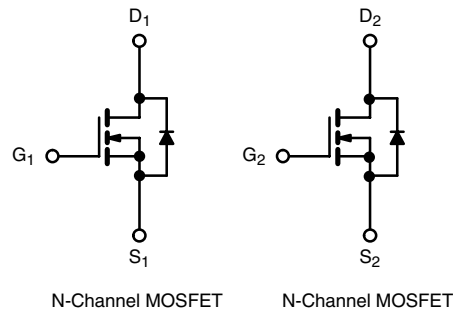
RoHS COMPLIANT

APPLICATIONS

- Primary Side Switch
- Synchronous Rectification



Ordering Information: Si7216DN-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	40	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	6 ^e	A
	T _C = 70 °C		5 ^e	
	T _A = 25 °C		6.5 ^{a, b}	
	T _A = 70 °C		5.2 ^{a, b}	
Pulsed Drain Current		I _{DM}	20	A
Continuous Source-Drain Diode Current		I _S	6 ^e	
				2.0 ^{a, b}
Avalanche Current		I _{AS}	10	mJ
Single-Pulse Avalanche Energy		E _{AS}	5	
Maximum Power Dissipation	T _C = 25 °C	P _D	20.8	W
	T _C = 70 °C		13.3	
	T _A = 25 °C		2.5 ^{a, b}	
	T _A = 70 °C		1.6 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}			260	

Notes:

- Surface Mounted on 1" x 1" FR4 Board.
- t = 10 sec.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Package limited.

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10 \text{ sec}$	R_{thJA}	38	50	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.5	6	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
 b. Maximum under steady state conditions is 94 °C/W.

SPECIFICATIONS ($T_J = 25 \text{ °C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \text{ }\mu\text{A}$		43		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \text{ }\mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.025	0.032	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$		0.031	0.039	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ A}$		25		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		670		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			50		
Total Gate Charge	Q_g	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		12.5	19	nC
		$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		5.5	8.5	
Gate-Source Charge	Q_{gs}			2		
Gate-Drain Charge	Q_{gd}			2		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		3.4	5.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20 \text{ V}, R_L = 4 \text{ }\Omega$ $I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \text{ }\Omega$		16	25	ns
Rise Time	t_r			142	215	
Turn-Off Delay Time	$t_{d(off)}$			16	25	
Fall Time	t_f			7	12	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20 \text{ V}, R_L = 4 \text{ }\Omega$ $I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \text{ }\Omega$		9	15	
Rise Time	t_r			57	90	
Turn-Off Delay Time	$t_{d(off)}$			19	30	
Fall Time	t_f			5	10	



SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			6	A
Pulse Diode Forward Current ^a	I _{SM}				20	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs, T _J = 25 °C		50	75	ns
Body Diode Reverse Recovery Charge	Q _{rr}			40	60	nC
Reverse Recovery Fall Time	t _a				35	ns
Reverse Recovery Rise Time	t _b				15	

Notes

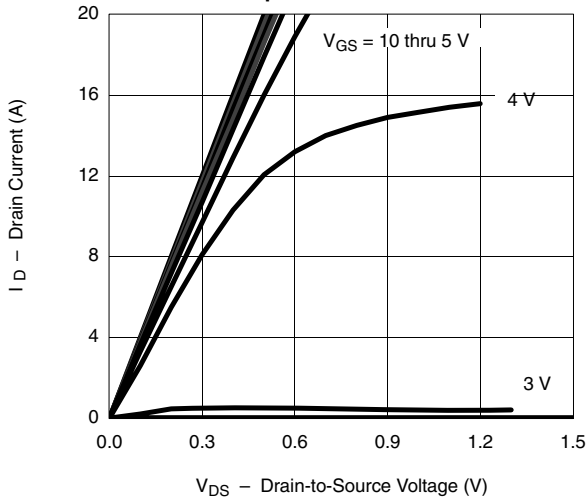
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

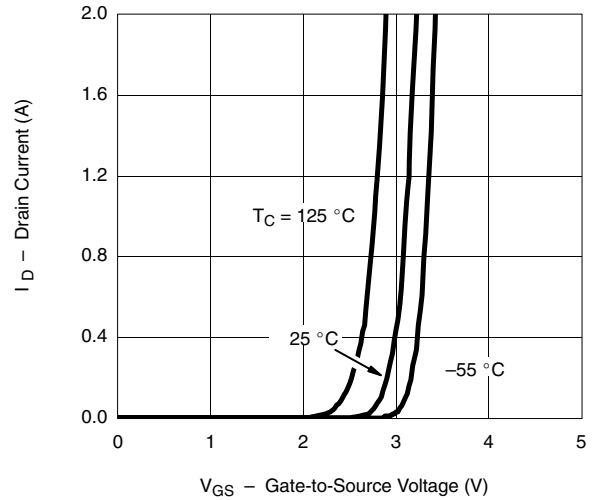


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

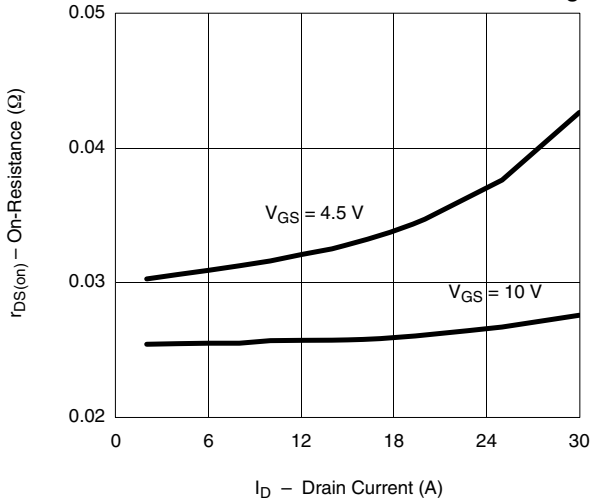
Output Characteristics



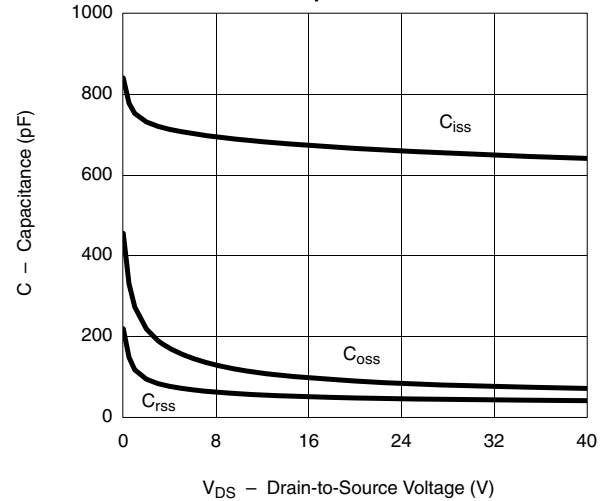
Transfer Characteristics



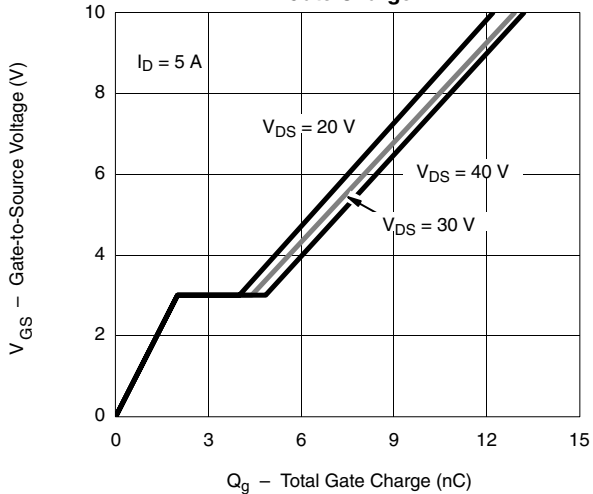
On-Resistance vs. Drain Current and Gate Voltage



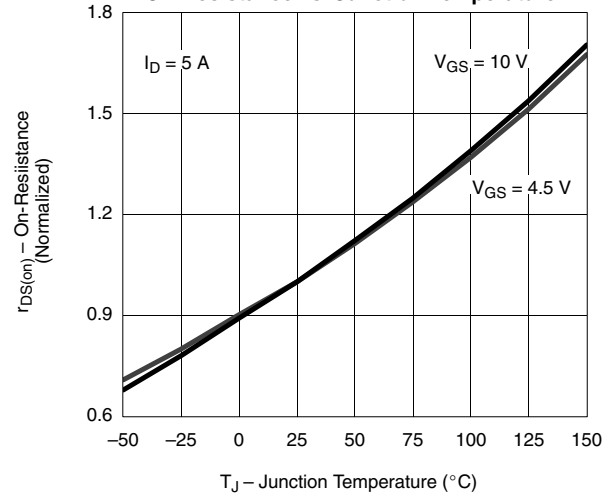
Capacitance



Gate Charge



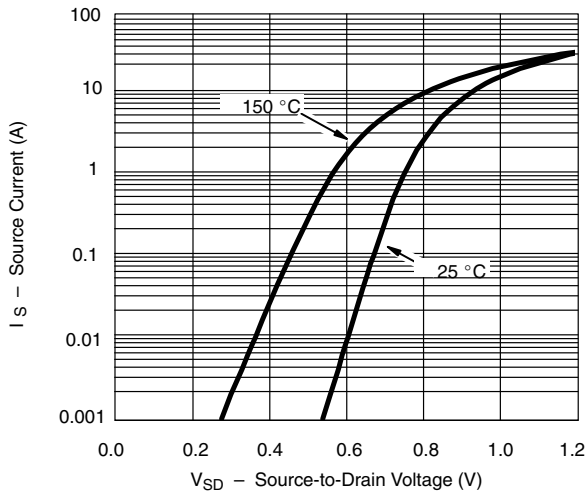
On-Resistance vs. Junction Temperature



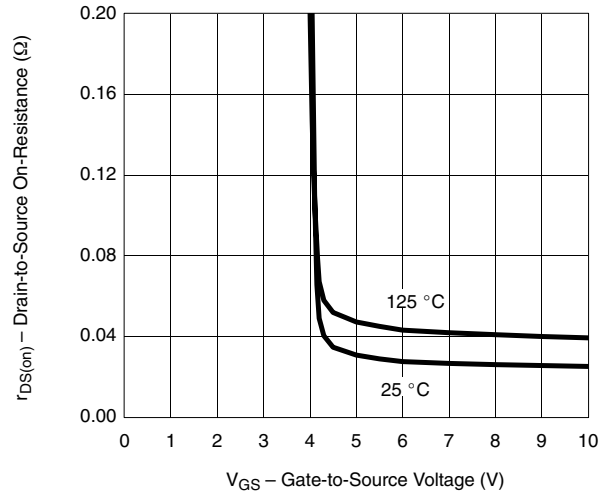


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

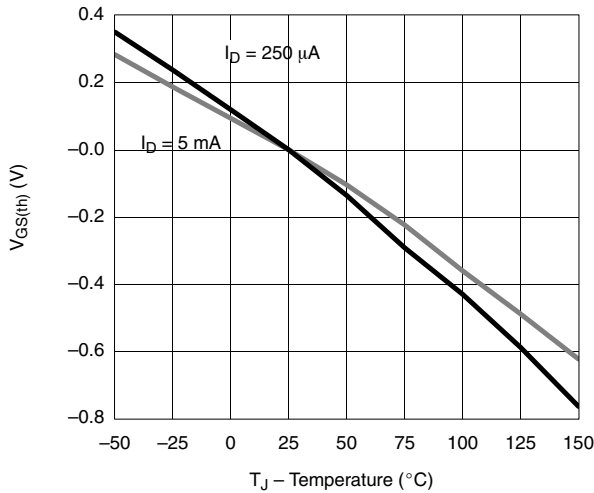
Source-Drain Diode Forward Voltage



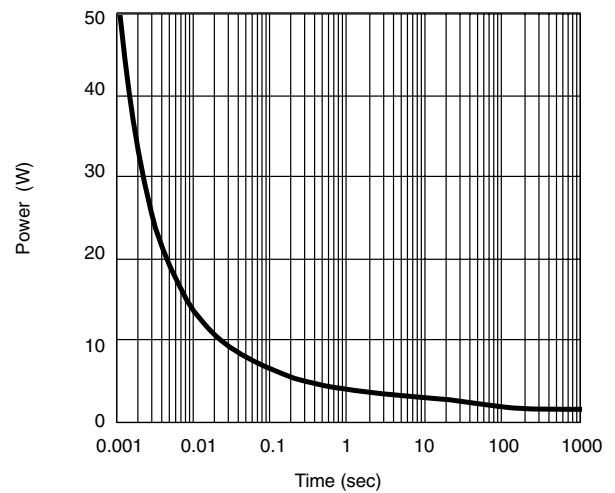
On-Resistance vs. Gate-to-Source Voltage



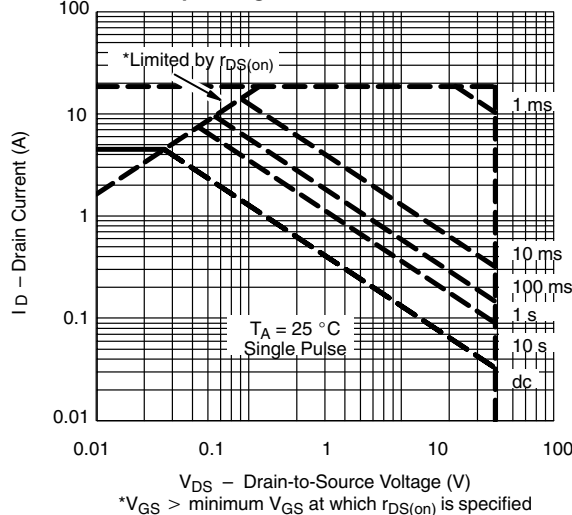
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

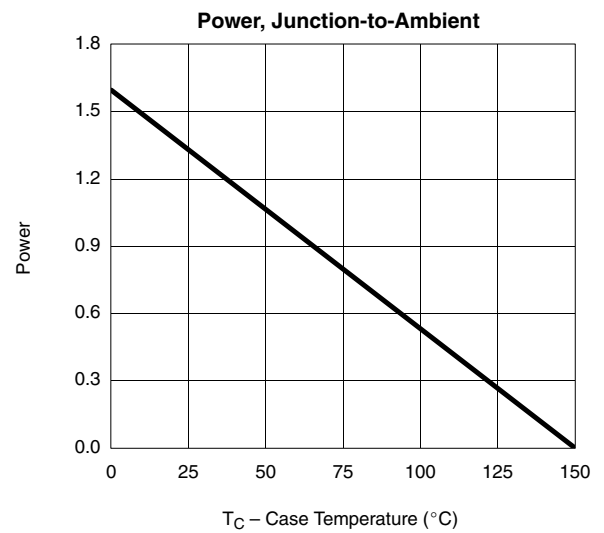
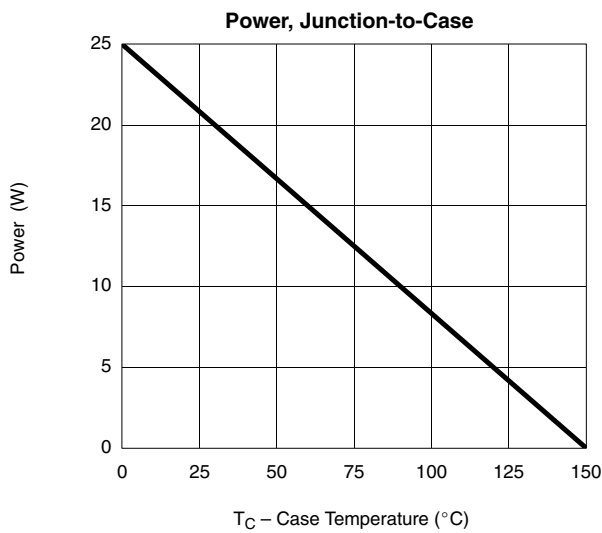
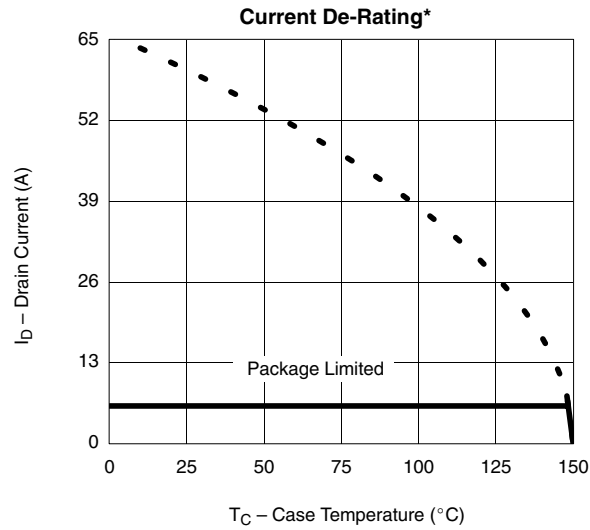


Safe Operating Area, Junction-to-Ambient





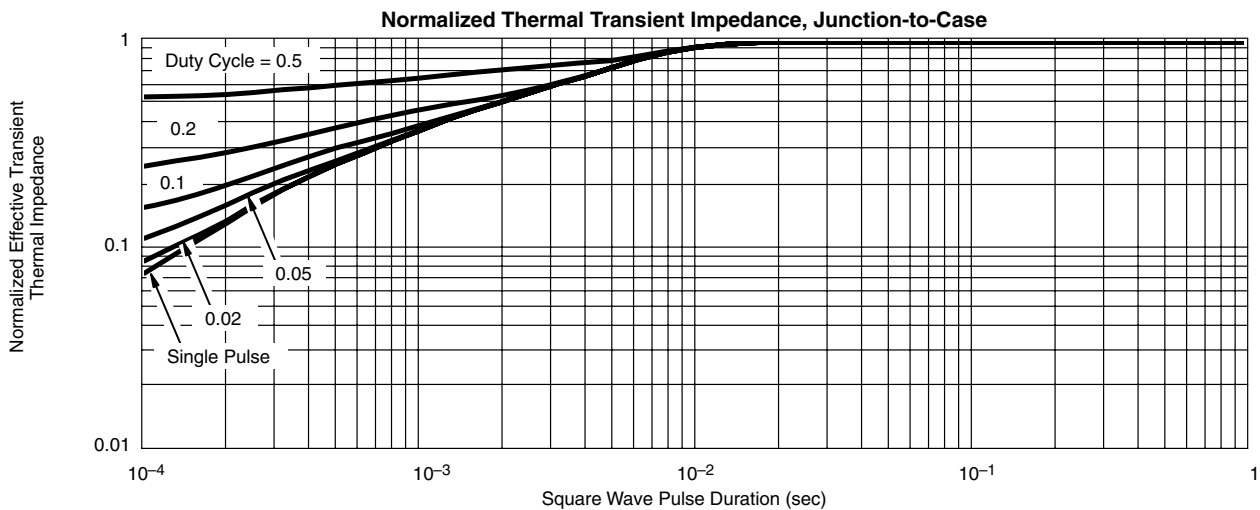
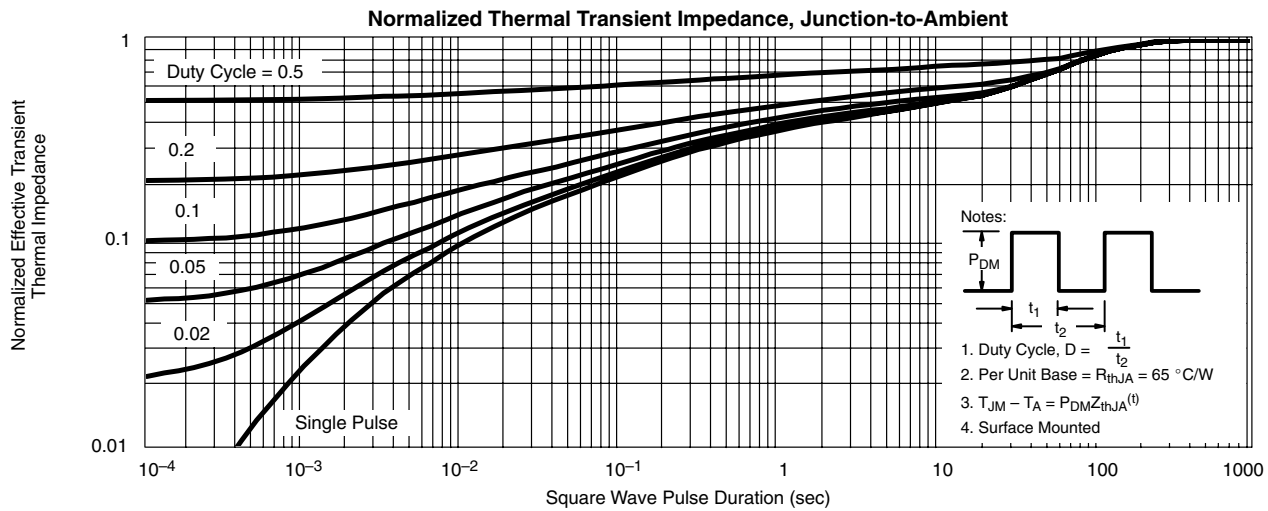
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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